SQ610

IP Surveillance Device SoC

Brief Specification

Version 1.1 – Nov 8th, 2004

SERVICE & QUALITY TECHNOLOGY CO., LTD.

6F, No.150, Sec.4 Chengde Rd., Shrlin Chiu, Taipei, Taiwan 111, R.O.C.

Tel: 886-2-66111177 Fax: 886-2-66106777

http://www.sq.com.tw/

REVISION HISTORY

Document NO: BE046101

REVISION #	DATE	DESCRIPTION	PAGE
Version 1.0	Aug. 19th, 2004	Formal release	
Version 1.1	Nov 8th, 2004	1. Revise 1.2 Features: add a "†" mark on the description of CCIR656 decoder	32
		2. Revise 1.2 Features: Add the supporting feature, CCIR656 decoder supported by the SQ610D, in the note	32
		3. Revise Table 2-4: modify the pin descriptions of A1 and A2	42
		4. Revise Table 2-13: mdify the pin description of ADC_datain[9:0]	45

1 INTRODUCTION

1.1 General Description

The SQ610 is a feature-optimized and cost-effective IP surveillance device controller that offers true SoC capability. It combines CPU, sensor control, image processor, GPU, JPEG CODEC and Ethernet MAC on a single chip. The SQ610 can interface to both CCD and CMOS sensors up to 2.1 million pixels resolutions. Another grand feature is that it comes with TCP/IP protocol stack and RTOS software development kit that supports DDNS and DHCP client protocol to connect with dynamic IP for web browsing and it is enriched by SMTP, FTP, as well as PPPoE service. Besides connecting to a PC, the SQ610 supports real-time video display on TV screen in either NTSC or PAL format. In addition, it provides high throughput SDRAM controller, on board flash memory interface and memory card controller for code, file or image storage. It also supports AC'97 CODEC for audio function and CCIR656 decoder for the requirement of digital CCTV segment.

For both IP camera and surveillance device manufactures, the SQ610 is an integral solution providing better speed and performance but great cost effectiveness. It satisfies the consumers' demands on remote image capturing and real time monitoring via only an internet browser in an IP based environments.

1.2 Features

- Image Frame Rate
  - 30 fps for CIF/QCIF/QVGA resolution
  - 10 fps for VGA resolution
- Image Capture
  - Supports 1/3" and 1/4" CMOS sensor
  - Supports 1/3" and 1/4" CCD sensor
  - Supports up to 2.1M pixels
  - Supports ITU-R CCIR656 decoder input†
- JPEG / Motion JPEG Compression
  - Embedded JPEG CODEC
  - Built-in JPEG encoder by 4:2:2 and 4:2:0 sampling
  - Supports multi-level JPEG compression ratio by changing quantization scale
- Motion Image Resolution
  - 640 × 480, 320 × 240, 160 × 120 (typically)
- Image Processing
  - Supports Auto Exposure (AE)
  - Supports Auto White Balance (AWB)
  - Supports Auto Gain Control (AGC)

- Network Access
  - Embedded IEEE 802.3 compliant 10/100 Mbps Ethernet MAC
  - Media Independent Interface (MII)
  - Provides PCMCIA host interface for 802.11x WLAN
- Networking Protocol
  - Support ARP/ICMP/TCP/IP/UDP
  - Support DDNS/DHCP
  - Support Http/PPPoE/FTP/SMTP allocation
- Audio†
  - Supports AC'97 audio controller for AC'97 CODEC
- Memory Card Controller
  - CF/Micro-drive/SD/MMC/SM/xD/Nand type Flash
- Display Interface
  - Embedded TV encoder for both NTSC and PAL composite video
  - Embedded TFT LCD controller
  - Supports real-time TV Monitoring
  - Supports H/W OSD function
  - Built-in segment LCD controller
  - Supports CCIR656 encoder output
- System Platform
  - Provides RTOS for maximum S/W stability and capability
  - Supports C++ embedded development system
- CPU
  - Supports external ROM up to 16MB
  - Supports 1M × 16, 4M × 16, 8M × 16 SDRAM
  - 32 PIOs for application control
  - System operation clock: 54 MHz
- External Control
  - Supports one RS-232 port for PTZ [Pan/Tilt/Zoom] camera control
  - Supports USB 1.1 device controller
  - Supports 16-bit PCMCIA host interface
  - Supports IDE HDD & CD-RW
- Power
  - Operation voltage range: 3.3 V
  - Power consumption: 420mA
- Supports triple-mode camera applications: Web camera DSC, PC camera, and TV camera

† *The AC'97 audio controller and the CCIR656 decoder are supported by SQ610D only.*

1.3 Applications

- IP CAM
- IP Video Server
- Web Server
- IP DVR
- Real-time Remote Monitoring
- Value-added IP Surveillance Device

2 SYSTEM OVERVIEW

The SQ610 consists of an Ethernet MAC, a PCMCIA host interface, an USB1.1 device controller, an image processor, a scalar, a CCIR656 CODEC, a JPEG CODEC, an AC'97 audio controller, a SDRAM controller, a memory card interface, a GPU, an OSD controller, a TV encoder and a TFT LCD controller. Figure 2-1 shows the system block diagram.

2.1 System Block Diagram

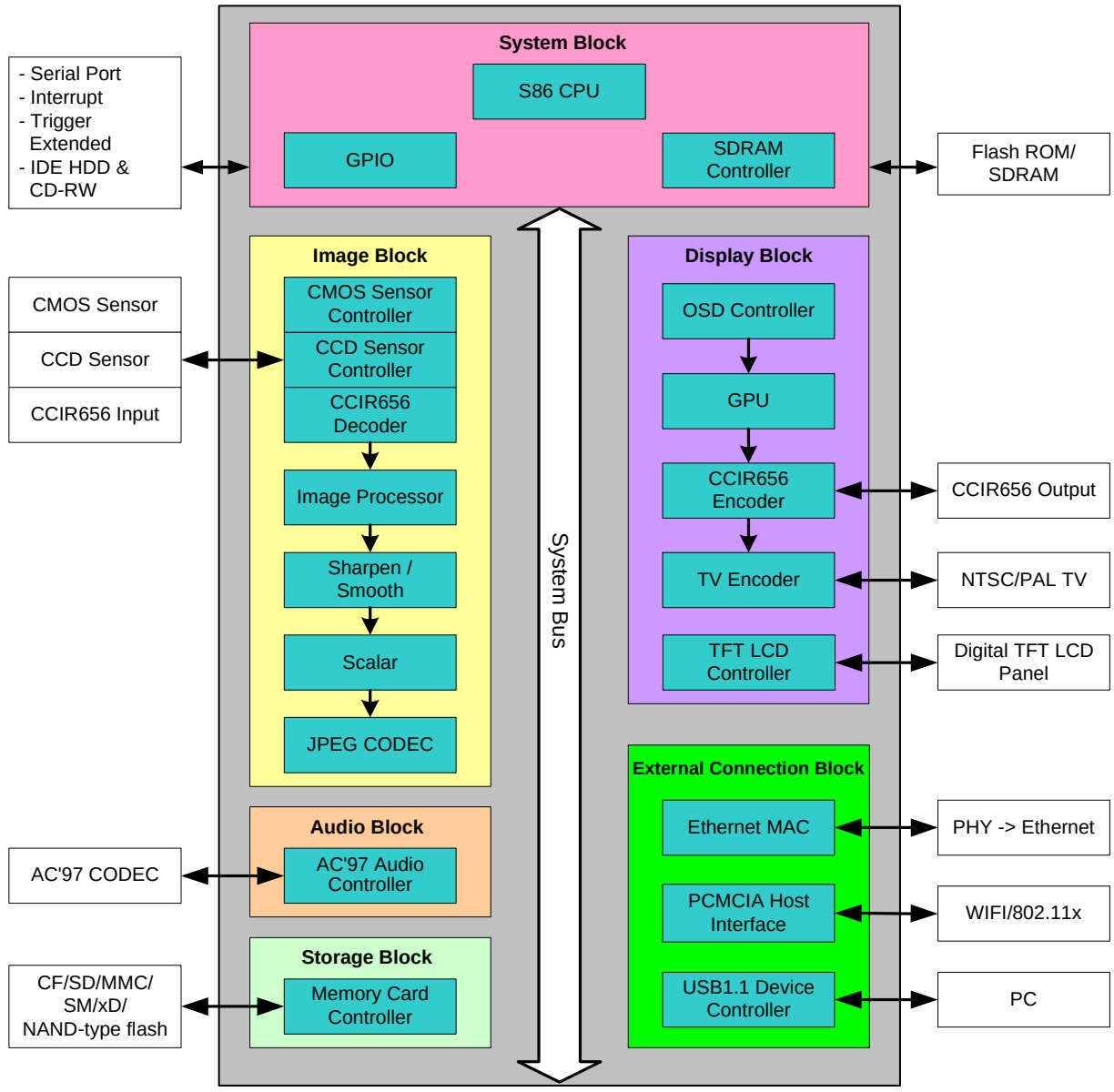


FIGURE 2–1: SQ610 SYSTEM BLOCK DIAGRAM

2.2 System Architecture

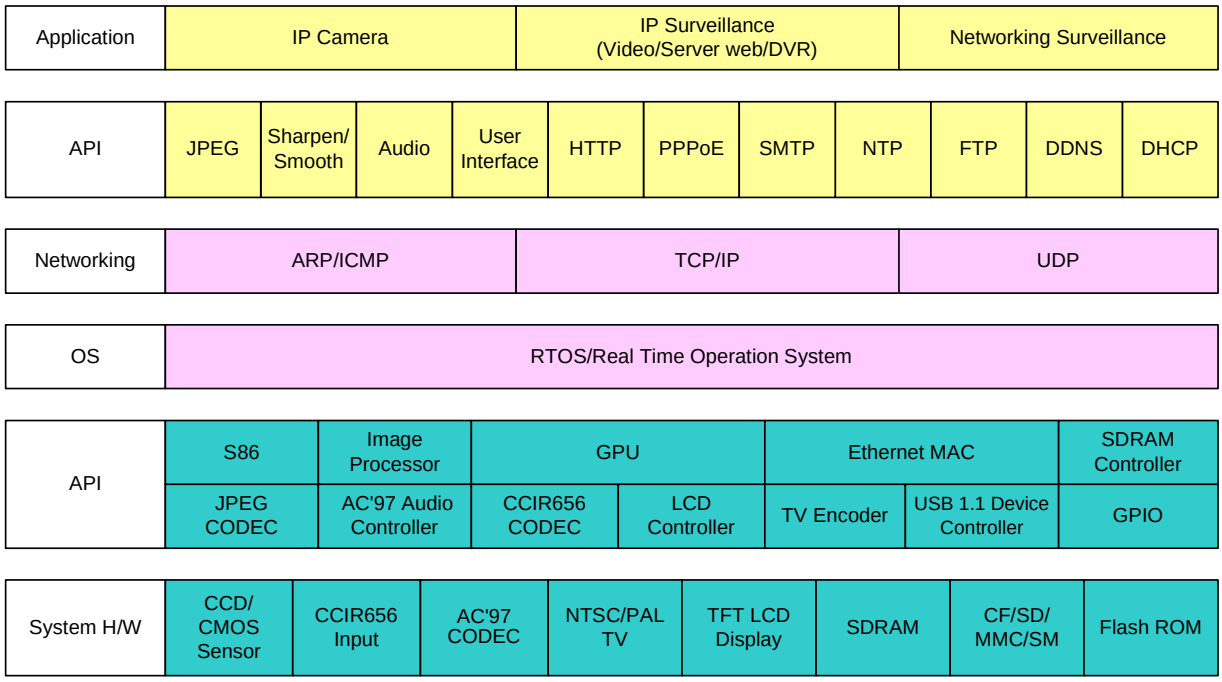


FIGURE 2–2: SQ610 SYSTEM ARCHITECTURE

2.3 Pin Information

2.3.1 Pin Assignment

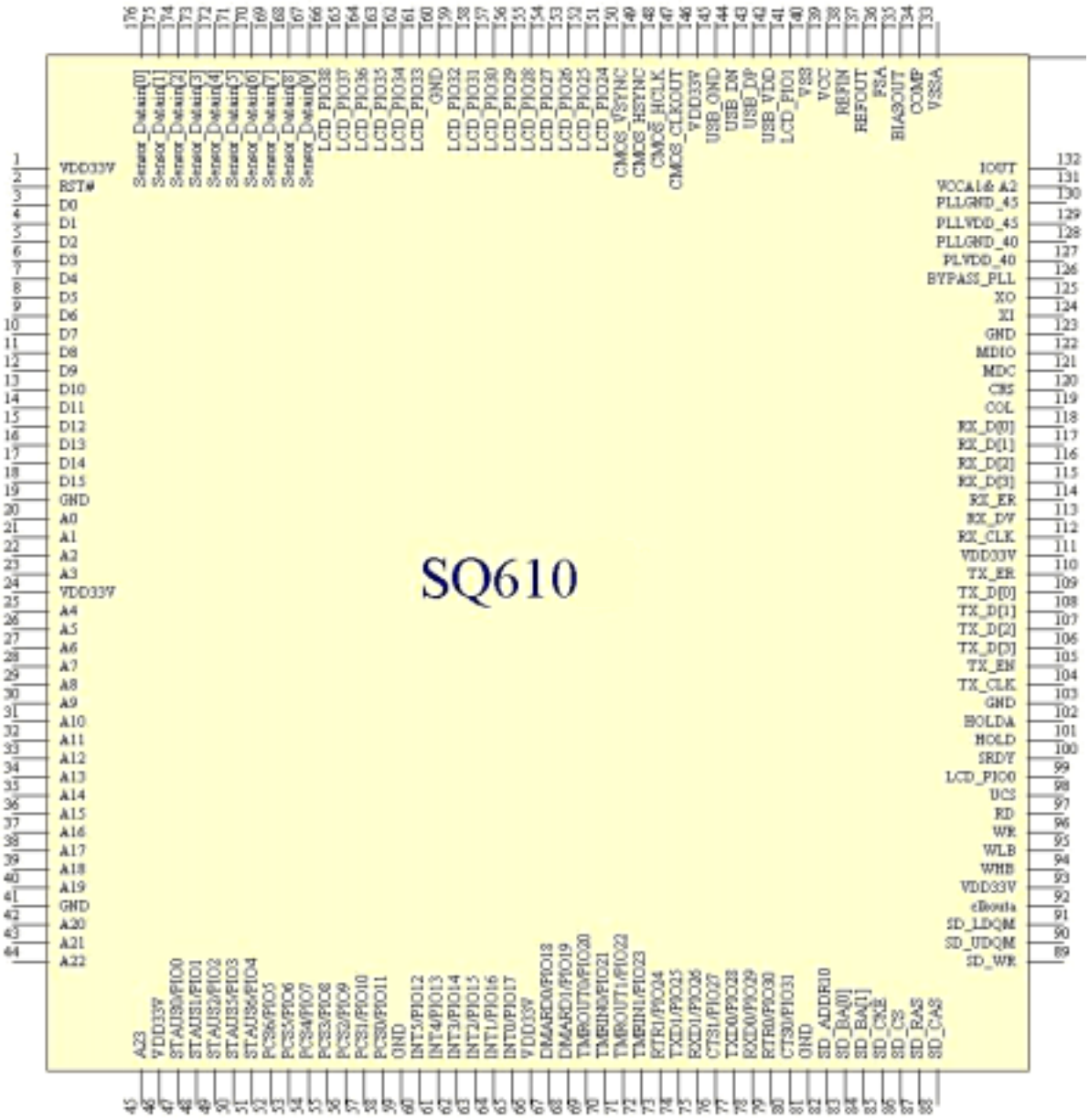


FIGURE 2–3: SQ610 PIN ASSIGNMENT

2.3.2 Pin List

TABLE 2–1:PIN LIST

PIN NO	NAME	PIN NO	NAME
1	VDD	**36**	ADDR15/PC_ADDR15
2	RST	**37**	ADDR16/PC_ADDR16
3	DATA0/PC_DATA0	**38**	ADDR17/PC_ADDR17
4	DATA1/PC_DATA1	**39**	ADDR18/PC_ADDR18
5	DATA2/PC_DATA2	**40**	ADDR19/PC_ADDR19
6	DATA3/PC_DATA3	**41**	GND
7	DATA4/PC_DATA4	**42**	ADDR20/LCD_PIO20
8	DATA5/PC_DATA5	**43**	ADDR21/LCD_PIO21
9	DATA6/PC_DATA6	**44**	ADDR22/LCD_PIO22
10	DATA7/PC_DATA7	**45**	ADDR23/LCD_PIO23
11	DATA8/PC_DATA8	**46**	VDD
12	DATA9/PC_DATA9	**47**	PIO0/STATUS0/SCLK/Flash_CLE
13	DATA10/PC_DATA10	**48**	PIO1/STATUS1/SDIN/Flash_RE_n
14	DATA11/PC_DATA11	**49**	PIO2/STATUS2/SDOUT/Falsh_WR_n
15	DATA12/PC_DATA12	**50**	PIO3/STATUS5/SDEN0/Falsh_ALE
16	DATA13/PC_DATA13	**51**	PIO4/STATUS6/SDEN1/Falsh_WP_n
17	DATA14/PC_DATA14	**52**	PIO5/PCS6/PC_ADDR20/DCLK
18	DATA15/PC_DATA15	**53**	PIO6/PCS5/PC_ADDR21/RGB_DCLK0
19	GND	**54**	PIO7/PCS4/PC_ADDR22/RGB_DCLK1
20	ADDR0/PC_ADDR0	**55**	PIO8/PCS3/PC_ADDR23/RGB_DCLK2
21	ADDR1/PC_ADDR1	**56**	PIO9/PCS2/RGB_DCLK3
22	ADDR2/PC_ADDR2	**57**	PIO10/PCS1/RGB_DCLK4
23	ADDR3/PC_ADDR3	**58**	PIO11/PCS0/RGB_DCLK5
24	VDD33	**59**	GND
25	ADDR4/PC_ADDR4	**60**	PIO12/INT5
26	ADDR5/PC_ADDR5	**61**	PIO13/INT4
27	ADDR6/PC_ADDR6	**62**	PIO14/INT3/PC_ADDR24/HSYNC_DCLK
28	ADDR7/PC_ADDR7	**63**	PIO15/INT2/PC_ADDR25/VSYNC_DCLK
29	ADDR8/PC_ADDR8	**64**	PIO16/INT1/Flash_R_B
30	ADDR9/PC_ADDR9	**65**	PIO17/INT0/Flash_CD
31	ADDR10/PC_ADDR10	**66**	VDD
32	ADDR11/PC_ADDR11	**67**	PIO18/DMARQ0/Flash_data0
33	ADDR12/PC_ADDR12	**68**	PIO19/DMARQ1/Flash_data1
34	ADDR13/PC_ADDR13	**69**	PIO20/TMROUT0/Flash1_ce_n
35	ADDR14/PC_ADDR14	**70**	PIO21/TMRIN0/Flash2_ce_n

PIN NO	NAME	PIN NO	NAME
71	PIO22/TMROUT1/Flash_data2	**106**	MIITXD3/CE2/LCD_PIO4/SL_charge_enb
72	PIO23/TMRIN1/Flash_data3	**107**	MIITXD2/RESET/LCD_PIO5
73	PIO24/RTR1/Vcc_3_EN	**108**	MIITXD1/REG/LCD_PIO6
74	PIO25/TXD1	**109**	MIITXD0/OE/LCD_PIO7
75	PIO26/RXD1	**110**	TX_ER/WE/LCD_PIO8
76	PIO27/CTS1/Vcc_5_EN	**111**	VDD
77	PIO28/TXD0/Flash_data4	**112**	MIIRX_CLK/STSCHG/LCD_PIO9
78	PIO29/RXD0/Flash_data5	**113**	MIIRX_DV/SPKR/LCD_PIO10
79	PIO30/RTR0/Flash_data6	**114**	MIIRX_ER/VS1/LCD_PIO11
80	PIO31/CTS0/Flash_data7	**115**	MIIRXD3/VS2/LCD_PIO12
81	GND	**116**	MIIRXD2/CD1/LCD_PIO13
82	SD_ADDR10	**117**	MIIRXD1/CD2/LCD_PIO14
83	SD_BA0	**118**	MIIRXD0/WAIT/LCD_PIO15
84	SD_BA1	**119**	MIICOL/INPACK/LCD_PIO16
85	SD_CKE	**120**	MIICRS/IOIS16/LCD_PIO17
86	SD_CS	**121**	MDC/IORD/LCD_PIO18
87	SD_RAS	**122**	MDIO/IOWR/LCD_PIO19
88	SD_CAS	**123**	GND
89	SD_WR	**124**	XI
90	SD_UDQM	**125**	XIO
91	SD_LDQM	**126**	BYPASS_PLL
92	clkouta	**127**	PLLVDD_40
93	VDD	**128**	PLLGND_40
94	WHB/AC97_sync	**129**	PLLVDD_45
95	WLB/AC97_reset_n	**130**	PLLGND_45
96	WR	**131**	VDDA
97	RD	**132**	IOUT
98	UCS	**133**	VSSA
99	LCD_PIO0	**134**	COMP
100	SRDY/AC97_bit_clk	**135**	BIASOUT
101	HOLD/AC97_data_in	**136**	FSA
102	HOLDA/AC97_data_out	**137**	REFOUT
103	GND	**138**	REFIN
104	TX_CLK/IREQ/LCD_PIO2/ segment2	**139**	VCC
105	TX_EN/CE1/LCD_PIO3/SL_trigger	**140**	VSS

PIN NO	NAME	PIN NO	NAME
141	LCD_PIO1	**159**	LCD_PIO32/CCD_FH2
142	USB_VDD	**160**	GND
143	USB_DP	**161**	LCD_PIO33/CCD_PG1
144	USB_DN	**162**	LCD_PIO34/CCD_PG2
145	USB_GND	**163**	LCD_PIO35/CCD_SUBI
146	VDD	**164**	LCD_PIO36/ADC_sh1
147	cmos_clkout/ADC_clk	**165**	LCD_PIO37/ADC_sh2
148	cmos_hclk/ADC_sclk	**166**	LCD_PIO38/ADC_preblack
149	cmos_hsync/ADC_clamp	**167**	sensor_datain9/ADC_datain9
150	cmos_vsync/ADC_CAL	**168**	sensor_datain8/ADC_datain8/clkin_656
151	LCD_PIO24/ADC_load	**169**	sensor_datain7/ADC_datain7/dain_656[7]
152	LCD_PIO25/ADC_sdi	**170**	sensor_datain6/ADC_datain6/dain_656[6]
153	LCD_PIO26/CCD_BI1	**171**	sensor_datain5/ADC_datain5/dain_656[5]
154	LCD_PIO27/CCD_BI2	**172**	sensor_datain4/ADC_datain4/dain_656[4]
155	LCD_PIO28/CCD_TI1	**173**	sensor_datain3/ADC_datain3/dain_656[3]
156	LCD_PIO29/CCD_TI2	**174**	sensor_datain2/ADC_datain2/dain_656[2]
157	LCD_PIO30/CCD_RG	**175**	sensor_datain1/ADC_datain1/dain_656[1]
158	LCD_PIO31/CCD_FH1	**176**	sensor_datain0/ADC_datain0/dain_656[0]

2.3.3 Pin Descriptions

TABLE 2–2: POWER SUPPLY PINS

PIN NO	NAME	I/O	DESCRIPTION
1	VDD	PWR	Power, Digital VDD = 3.3V
19	GND	PWR	Ground
24	VDD	PWR	Power, Digital VDD = 3.3V
41	GND	PWR	Ground
46	VDD	PWR	Power, Digital VDD = 3.3V
59	GND	PWR	Ground
66	VDD	PWR	Power, Digital VDD = 3.3V
81	GND	PWR	Ground
93	VDD	PWR	Power, Digital VDD = 3.3V
103	GND	PWR	Ground
111	VDD	PWR	Power, Digital VDD = 3.3V
123	GND	PWR	Ground
127	PLLVDD_40	PWR	Power for PLL X 4, 3.3V
128	PLLGND_40	PWR	Ground for PLL X 4
129	PLLVDD_45	PWR	Power for PLL X 4.5, 3.3V
130	PLLGND_45	PWR	Ground for PLL X 4.5
131	VDDA	PWR	DAC Power, Analog VDD = 3.3V
133	VSSA	PWR	DAC Ground, Analog ground
139	VCC	PWR	DAC Power, Digital VDD = 3.3V
140	VSS	PWR	DAC Ground, Digital ground
142	USB_VDD	PWR	USB Power, Analog VDD = 3.3V
145	USB_GND	PWR	USB Ground, Analog ground
146	VDD	PWR	Power, Digital VDD = 3.3V
160	GND	PWR	Ground

TABLE 2–3: SYSTEM PINS

PIN NO	NAME	I/O	DESCRIPTION
2	RST	I	System reset, active low
124	XI	I	12MHz Crystal In
125	XO	I/O	12MHz Crystal Out
126	BYPASS_PLL	I	Bypass PLL function

TABLE 2–4: ADDRESS AND DATA PINS

PIN NO	NAME	I/O	DESCRIPTION
3 18	DATA0 DATA15	I/O	Data Bus[0:15]
20 23	A0 A3	I/O	Address Bus[0:3] A0: pull low for 16-bit ROM pull high for 8-bit ROM A1: pull low for operating at 48MHz frequency pull high for operating at 54MHz frequency A2: pull high for normal operation
25 36	A4 A15	O	Address Bus[4:15]
37~40	A16~A19	I/O	Address Bus[16:19] A16~A19: pull low for normal operation
42 45	A20 A23	O	Address Bus[20:23]

NOTE: The setting to A2 is only active on the SQ610D.

TABLE 2–5: SDRAM INTERFACE CONTROL PINS

PIN NO	NAME	I/O	DESCRIPTION
82	SD_ADDR10	O	SDRAM Address[10] Only SDRAM Address 10 is used.
83~84	SD_BA0 1	O	SDRAM Back Address[0:1] These two signals are used to determine which back is to be activated.
85	SD_CKE	O	SDRAM Clock Enable When SD_CKE is high, the SD CLK signal is activated; when it is low, the SD CLK signal is deactivated. Thus it initiates one of the following three modes: Power Down Mode, Suspend Mode, and Self Refresh Mode.
86	SD_CS	O	SDRAM Chip Select When SD_CS is low, the command decoder is enabled; when it is high, the command decoder is disabled. As long as the command decoder is disabled, all new commands will be ignored while the previous operations continue.
87	SD_RAS	O	SDRAM Row Address Select This signal is sampled at the positive clock rising edge, and is used to select the command to be executed.
88	SD_CAS	O	SDRAM Column Address Select
89	SD_WR	O	SDRAM Write Enable
90	SD_UDQM	O	SDRAM Upper Byte Data I/O Mask
91	SD_LDQM	O	SDRAM Lower Byte Data I/O Mask
92	clkouta	O	54MHz Clock Output to SDRAM

TABLE 2–6: CF/MICRO-DRIVE CARD INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
67~68	Flash_data0 ~ Flash_data1	I/O	CF data bus [0:1]
71~72	Flash_data2 ~ Flash_data3	I/O	CF data bus [2:3]
77~80	Flash_data4 ~ Flash_data7	I/O	CF data bus [4:7]
69	Flash1_ce_n	O	CF Chip Enable
47	Flash_CLE	O	CF DA0
48	Flash_RE_n	O	CF IORD
49	Flash_WR_n	O	CF IOWR
50	Flash_ALE	O	CF DA1
51	Flash_WP_n	O	CF DA2

TABLE 2–7: SM CARD INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
67~68	Flash_data0 ~ Flash_data1	I/O	SM data bus [0:1]
71~72	Flash_data2 ~ Flash_data3	I/O	SM data bus [2:3]
77~80	Flash_data4 ~ Flash_data7	I/O	SM data bus [4:7]
70	Flash2_ce_n	O	SM Chip Enable
47	Flash_CLE	O	SM Command Latch Enable
48	Flash_RE_n	O	SM Read Enable
49	Flash_WR_n	O	SM Write Enable
50	Flash_ALE	O	SM Address Latch Enable
51	Flash_WP_n	O	SM Write Protect
64	Flash_R_B	I	SM Ready Busy
65	Flash_CD	I	SM Card Detection

TABLE 2–8: SD/MMC CARD INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
47	SCLK	O	SD Card Clock
48	SDIN	I	SD Card I/F Data In
49	SDOUT	O	SD Card I/F Data Out
50	SDOE0	O	SD Card I/F Output Enable[0]
51	SDOE1	O	SD Card I/F Output Enable[1]

TABLE 2–9: AC'97 CONTROLLER PINS

PIN NO	NAME	I/O	DESCRIPTION
94	AC97_sync	O	AC–Link Synchronous This signal is used to provide the 48kHz fixed rate sample sync to AC'97.
95	AC97_reset_n	O	AC–Link Reset This signal is used to H/W reset the AC'97.
100	AC97_bit_clk	I	AC–Link Bit Clock This signal is the 12.288MHz serial data clock from AC'97.
101	AC97_data_in	I	AC–Link Data In This signal is the serial, time division multiplexed input stream from AC'97.
102	AC97_data_out	O	AC–Link Data Out This signal is used to input the serial, time division multiplexed stream to AC'97.

NOTE: These signals are only available on the SQ610D.

TABLE 2–10: USB (MSDC) CONTROLLER PINS

PIN NO	NAME	I/O	DESCRIPTION
143	USB_DP	Analog I/O	USB Data + Differential Bus
144	USB_DN	Analog I/O	USB Data – Differential Bus

TABLE 2–11: MAC MII INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
104	TX_CLK	I	MII Transmit Clock The transmit clock is sourced by an external PHY device with 25MHz or 2.5MHz, depended on the Ethernet speed.
105	TX_EN	O	MII Transmit Enable
106~109	TXD[3:0]	O	MII Transmit Data [3:0]
110	TX_ER	O	MII Transmit Error Indication
112	RX_CLK	I	MII Receive Clock The receive clock is sourced by an external PHY device with 25MHz or 2.5MHz, depended on the Ethernet speed.
113	RX_DV	I	MII Receive Valid
114	RX_ER	I	MII Receive Error Indication
115~118	RXD[3:0]	I	MII Receive Data [3:0]
119	COL	I	MII Collision Detection
120	CRS	I	MII Carrier Sense
121	MDC	O	MII Management Clock Output
122	MDIO	I/O	MII Management Data Input/Output

TABLE 2–12: CMOS SENSOR INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
147	cmos_clkout	O	CMOS Sensor Clock Output
148	cmos_hclk	I	CMOS Sensor Master Clock
149	cmos_hsync	I	CMOS Sensor Vertical Synchronization Signal
150	cmos_vsync	I	CMOS Sensor Horizontal Synchronization Signal
167~176	sensor_datain[9:0]	I	CMOS Sensor Image Data [9:0]

TABLE 2–13: CCD SENSOR INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
147	ADC_clk	O	ADC Data Clock Output
148	ADC_sclk	O	ADC 3-wire Serial Clock
149	ADC_clamp	O	ADC Clamp Pulse
150	ADC_CAL	O	ADC Blanking Pulse
151	ADC_load	O	ADC 3-wire Load Pulse
152	ADC_sdi	O	ADC 3-wire Data Input
153	CCD_BI1	O	CCD Vertical Shift 1 (2-phase)
154	CCD_BI2	O	CCD Vertical Shift 2 (2-phase)
155	CCD_TI1	O	CCD Vertical Shift 1 (3-phase)
156	CCD_TI2	O	CCD Vertical Shift 2 (3-phase)
157	CCD_RG	O	CCD Reset Gate Clock
158	CCD_FH1	O	CCD Horizontal clock 1
159	CCD_FH2	O	CCD Horizontal clock 2
161	CCD_PG1	O	CCD Vertical Shift 1 (3-phase pulse)
162	CCD_PG2	O	CCD Vertical Shift 2 (3-phase pulse)
163	CCD_SUBI	O	CCD Substrate Clock
164	ADC_sh1	O	ADC Sampling Position 1
165	ADC_sh2	O	ADC Sampling Position 2
166	ADC_preblack	O	ADC Block Level Period Pulse
167~176	ADC_datain[9:0]	I	CCD Sensor Image Data [9:0]

TABLE 2–14: CCIR656 DECODER INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
176~169	datain_656[7:0]	I	CCIR656 Decoder Data Input Bit 7~0
168	clkin_656	I	CCIR656 CLK Input (27MHz or 54MHz)

NOTES:
1. These signals are only available on the SQ610D.
2. CCIR656 CLK 54MHz is for projector and CLK 27MHz for other output devices.

TABLE 2–15: PCMCIA INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
3~18	PC_DATA0~ PC_DATA15	I/O	PCMCIA Data Bus Bit 0~15
20~23	PC_ADDR0~ PC_ADDR3	O	PCMCIA Address Bus Bit 0~3
25~40	PC_ADDR4~ PC_ADDR19	O	PCMCIA Address Bus Bit 4~19
52~55	PC_ADDR20~ PC_ADDR23	O	PCMCIA Address Bus Bit 20~23
62~63	PC_ADDR24~ PC_ADDR25	O	PCMCIA Address Bus Bit 24~25
104	IREQ	I	Interrupt Request This signal is asserted to inform the system that the PC card has an interrupt that needs servicing.
105	CE1	O	Card Enable 1
106	CE2	O	Card Enable 2
107	RESET	O	Card Reset
108	REG	O	Register Select This signal when asserted specifies access to attribute memory.
109	OE	O	Output Enable This signal is active low and is asserted during memory read transfers from PC cards.
110	WE	O	Write Enable This signal is active low and is asserted during memory write transfers from PC cards.
112	STSCHG	I	I/O Status Change This signal is used to report a card status change.
113	SPKR	I	Digital Audio Waveform This signal is used to send audio information to the system speaker.
114	VS1	I	Voltage Sense 1
115	VS2	I	Voltage Sense 2
116	CD1	I	Card Detect 1
117	CD2	I	Card Detect 2
118	WAIT	I	Wait This signal is used to extend standard cycle time.
119	INPACK	I	Input Port Acknowledge This signal is asserted during I/O read transfers from a PC card when it recognizes the address.

PIN NO	NAME	I/O	DESCRIPTION
120	IOIS16	I	I/O size is 16-bit. This signal is asserted during I/O read transfers from PC card, if the device size is 16 bits.
121	IORD	O	I/O Read Command
122	IOWR	O	I/O Write Command
73	Vcc_3_EN	O	3.3V Power Enable Control to PCMCIA Card (active high)
76	Vcc_5_EN	O	5V Power Enable Control to PCMCIA Card (active high)

TABLE 2–16: DIGITAL TFT LCD PANEL INTERFACE PINS

PIN NO	NAME	I/O	DESCRIPTION
52	DCLK	O	The dot clock of LCD panel
53~58	RGB_DCLK0~ RGB_DCLK5	O	The data input of LCD panel
62	HSYNC_DCLK	O	The horizontal sync signal of dot data.
63	VSYNC_DCLK	O	The vertical sync signal of dot data.

TABLE 2–17: GENERAL PURPOSE I/O PORT PINS

PIN NO	NAME	I/O	DESCRIPTION
47~58	PIO0~PIO11	I/O	S86 GPIO Port 0~11
60~65	PIO12~PIO17	I/O	S86 GPIO Port 12~17
67~80	PIO18~PIO31	I/O	S86 GPIO Port 18~31
99	LCD_PIO0	I/O	LCD_PIO Port 0
141	LCD_PIO1	I/O	LCD_PIO Port 1
104~110	LCD_PIO2~ LCD_PIO8	I/O	LCD_PIO Port 2~8
112~122	LCD_PIO9~ LCD_PIO19	I/O	LCD_PIO Port 9~19
42~45	LCD_PIO20~ LCD_PIO23	I/O	LCD_PIO Port 20~23
151~159	LCD_PIO24~ LCD_PIO32	I/O	LCD_PIO Port 24~32
161~166	LCD_PIO33~ LCD_PIO38	I/O	LCD_PIO Port 33~38

TABLE 2–18: STATUS LCD PINS

PIN NO	NAME	I/O	DESCRIPTION
99	segment0	O	Status LCD Segment 0
141	segment1	O	Status LCD Segment 1
104~110	segment2~ segment8	O	Status LCD Segment 2~8
112~118	segment9~ segment15	O	Status LCD Segment 9~15
119~122	BP0~BP3	I/O	Status LCD Backplane 0~3

TABLE 2–19: CCIR656 ENCODER PINS

PIN NO	NAME	I/O	DESCRIPTION
52	clk_tv	O	27MHz clock output
53~58	tv_dataout0~tv_dataout5	O	CCIR656 Data Output 0~5
62~63	tv_dataout6~tv_dataout7	O	CCIR656 Data Output 6~7
60	tv_hsync	I	HSYNC Input to GPU
61	tv_vsync	I	VSYNC Input to GPU

3 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

TABLE 3–1: ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Power Supply	-0.3	3.9	V
V_{IN3}	Input Voltage of 3.3V I/O	-0.3	VCC+0.3	V
V_{OUT3}	Output Voltage of 3.3V I/O	-0.3	VCC+0.3	V
T_{STG}	Storage Temperature	-40	150	℃

3.2 Operation Conditions

TABLE 3–2: OPERATION CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Power Supply	3.0	3.3	3.6	V
VIN3	Input Voltage of 3.3V with 5V Tolerance I/O	0	3.3	5.25	V
TJ	Junction Operating Temperature: Commercial	0	25	115	℃

3.3 DC Characteristics of 3.3V I/O Cells

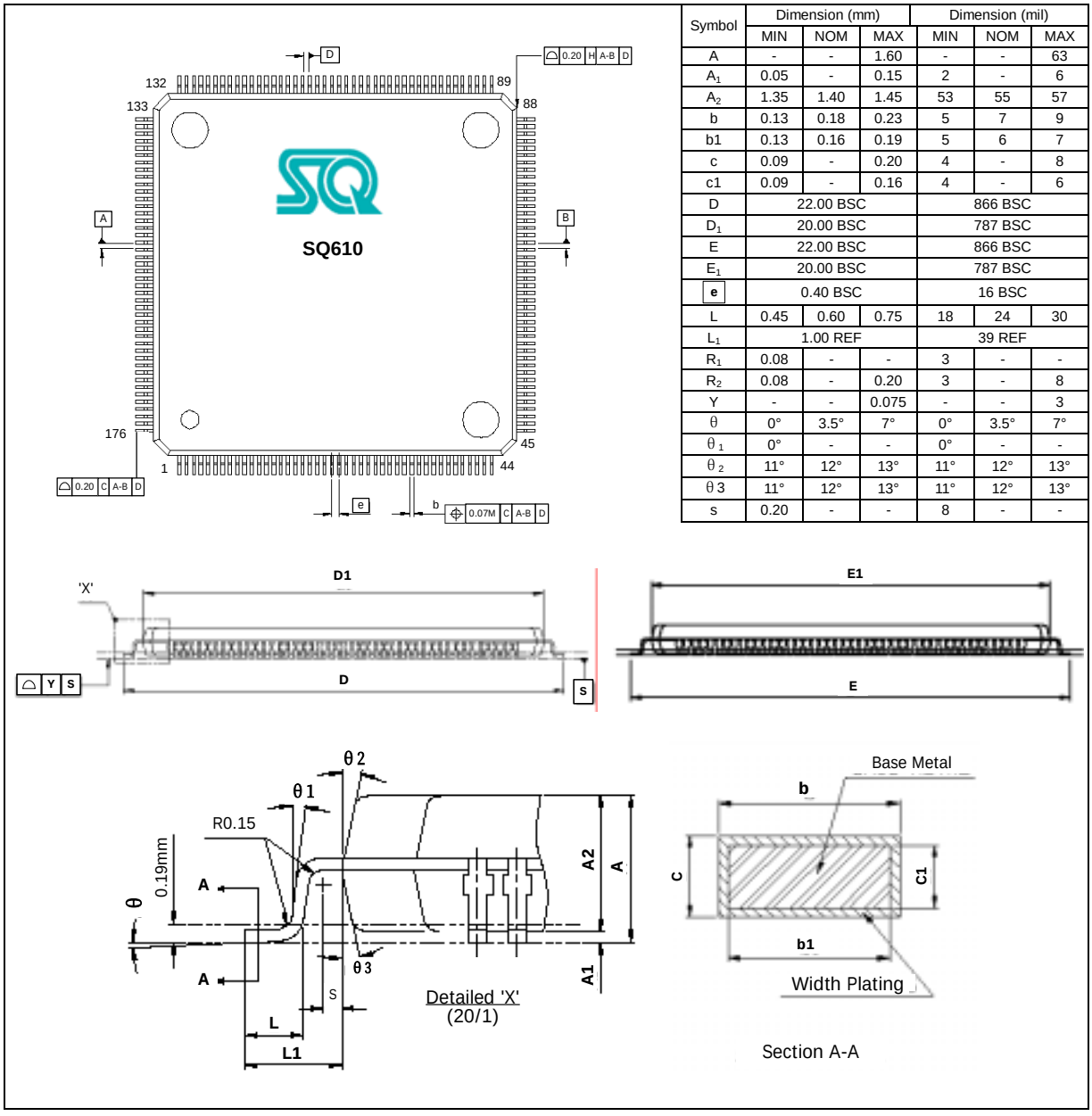
TABLE 3–3: DC CHARACTERISTICS OF 3.3V I/O CELLS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Power Supply	-	3.0	3.3	3.6	V
VIL	Input Low Voltage	CMOS	-	-	0.3*VCC	V
VIH	Input High Voltage	CMOS	0.7*VCC	-	-	V
VT-	Schmitt Trigger Negative Going	CMOS	0.9	1.2	-	V
VT+	Schmitt Trigger Positive Going Threshold	CMOS	-	2.1	2.5	V
VOL	Output Low Voltage	IOl = 4 mA	-	-	0.4	V
VOH	Output High Voltage	IOH = -4 mA	2.4	-	-	V

4 PACKAGING

4.1 LQFP 176-pin Package

Body size: 20*20*1.4mm



Symbol	Dimension (mm)			Dimension (mil)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	63
A_1	0.05	-	0.15	2	-	6
A_2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	7
c	0.09	-	0.20	4	-	8
c1	0.09	-	0.16	4	-	6
D	22.00 BSC			866 BSC		
D_1	20.00 BSC			787 BSC		
E	22.00 BSC			866 BSC		
E_1	20.00 BSC			787 BSC		
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L_1	1.00 REF			39 REF		
R_1	0.08	-	-	3	-	-
R_2	0.08	-	0.20	3	-	8
Y	-	-	0.075	-	-	3
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	-	-	0°	-	-
θ_2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20	-	-	8	-	-

FIGURE 4–1: LQFP 176-PIN PACKAGE DIAGRAM

NOTES:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm. Per side D1 and E1 are maximum plastic body size dimension including mold mismatch.
2. Dimension b does not include DAMBAR protrusion. Allowable DAMBAR protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

4.2 Ordering Information

TABLE 4–1: ORDERING INFORMATION TABLE

TYPE NO	PACKAGE	DESCRIPTION
SQ610C	LQFP176	Low-profile Quad Flat Package, 176-pin
SQ610D	LQFP176	Low-profile Quad Flat Package with Audio and CCIR656 decoder, 176-pin

4.3 Feature Comparison between SQ610C and SQ610D

TABLE 4–2: FEATURE COMPARISON TABLE

FEATURE	SQ610C	SQ610D
S86 CPU	✓	✓
SDRAM controller	✓	✓
CMOS sensor controller	✓	✓
CCD sensor controller	✓	✓
CCIR656 decoder	Not support	✓
Image gain controller	✓	✓
Image interpolation	✓	✓
Image accumulator	✓	✓
Image sharpen/smooth	✓	✓
Image pseudo sensor	✓	✓
Image scalar	✓	✓
JPEG CODEC	✓	✓
GPU	✓	✓
OSD controller	✓	✓
TV encoder	✓	✓
TFT LCD controller	✓	✓
Segment LCD controller	✓	✓
CCIR656 encoder	✓	✓
Ethernet MAC	✓	✓
PCMCIA host interface	✓	✓
AC'97 audio controller	Not support	✓
Memory card interface	✓	✓
USB device controller	✓	✓