Clock Generator with Integrated Buffers for Intel Pentium II Designs

FEATURES

- Multiple CPU clocks for SDRAM architecture of Pentium compatible systems
- Supports 2 Synchronous CPU clocks
- Supports 14 Synchronous SDRAM clocks
- Supports 6 Synchronous/Asynchronous PCI BUS clocks
- Supports 24 MHz floppy clock and 48MHz USB clock
- Provides POWER DOWN mode in slowing down CPU clock
- Spectrum Modulation reduce EMI
- Provides programmable clocks
- Provides I^2C interface
- 48 Pin SSOP package

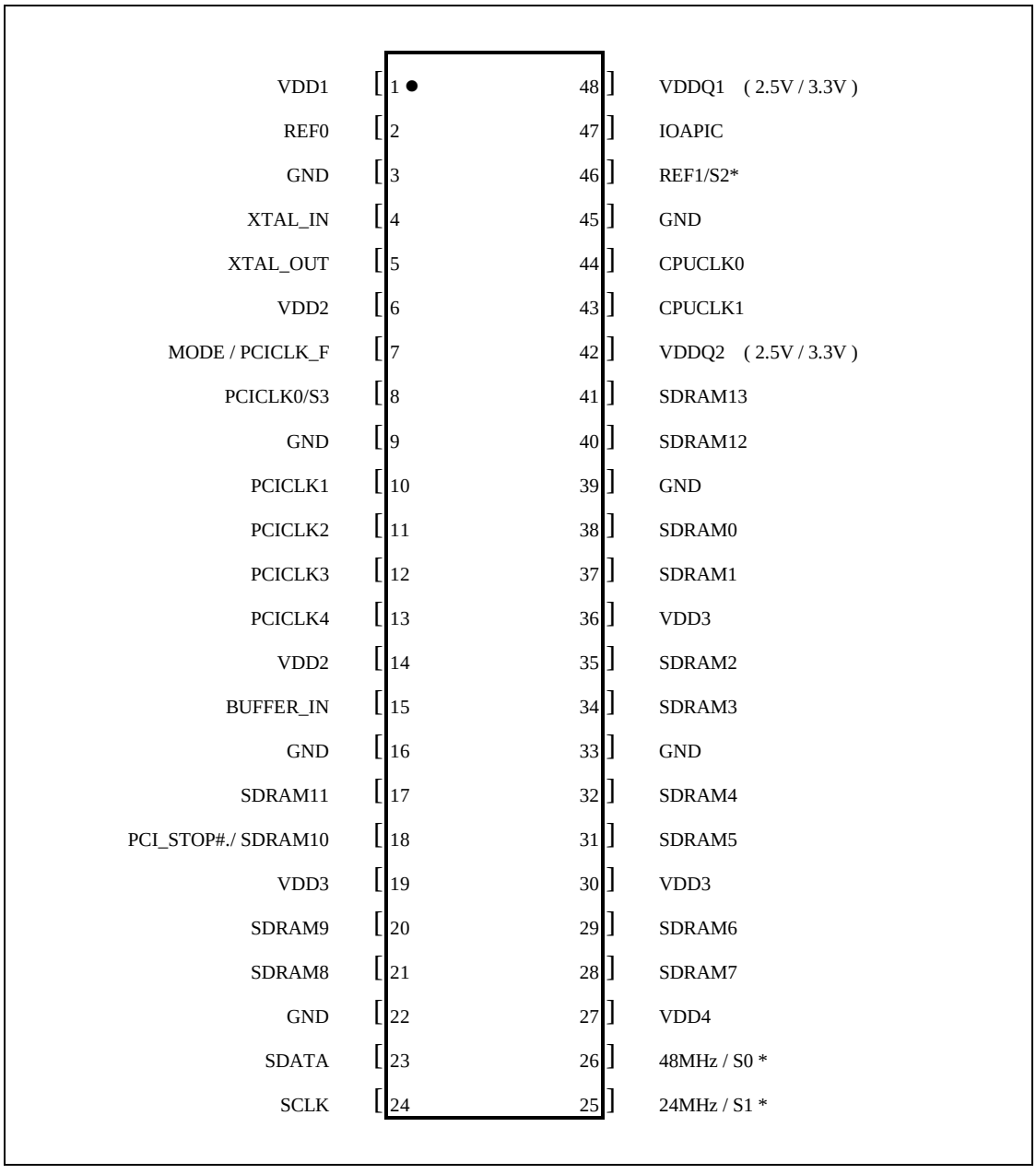
SELECT				CPU	PCI	48 MHz	24MHz	REF
S3	S2	S1	S0					IOAPIC
0	0	0	0	124	41.3 (CPU/3)	48	24	14.318
0	0	0	1	75	37.5 (CPU/2)	48	24	14.318
0	0	1	0	83.3	41.7 (CPU/2)	48	24	14.318
0	0	1	1	66.8	33.4 (CPU/2)	48	24	14.318
0	1	0	0	103	34.3 (CPU/3)	48	24	14.318
0	1	0	1	***112***	***37.3 (CPU/3)***	48	24	14.318
0	1	1	0	***133.3***	***33.3 (CPU/4)***	48	24	14.318
0	1	1	1	100	33.3 (CPU/3)	48	24	14.318
1	X	X	X	***133.3***	***33.3 (CPU/4)***	48	24	14.318

Notice:

* S0, S1, S2, S3, MODE are selected during Power-on.

PIN CONFIGURATION

RTM520-39



Notice:

S2, S1, S0 S3 are pulled high with 50K ohm at default.

Pin Descriptions

Pin Number	Pin Name	Type	Descriptions
2	REF0	OUT	Reference clock 14.31818MHz
4	XTAL_IN	IN	Crystal input, 14.31818 MHz
5	XTAL_OUT	OUT	Crystal output, 14.31818 MHz
7	PCICLK_F	OUT	Free running PCI clock
	MODE	IN	Power management
8	PCICLK0	OUT	Free running PCI clock
	S3	IN	Frequency selects for CPU and SDRAM clocks
10,11,12,13	PCLK 1..4	OUT	PCI clock outputs
15	Buffer in	IN	SDRAM clock reference input
17,18,20,21 28,29,31,32 34,35,37,38 40,41	SDRAM 13..0	OUT	SDRAM clock outputs
18	PCI_STOP#	IN	PCI clocks stop control
23	SDATA	Bi_dir	Serial data of I^2C bus
24	SCLK	IN	Serial clock of I^2C bus
25	24 MHz	OUT	24 MHz clock output
	S1	IN	Frequency selects for CPU and SDRAM clocks
26	48 MHz	OUT	48 MHz clock output
	S0	IN	Frequency selects for CPU and SDRAM clocks
43,44	CPUCLK 1..0	OUT	CPU clock outputs
46	REF1	OUT	Reference clock 14.31818MHz
	S2	IN	Frequency selects for CPU and SDRAM clocks
47	IOAPIC	OUT	IOAPIC clock output
1	VDD1	PWR	Power Supply 3.3V ϒ 5 %
6,14	VDD2	PWR	I/O Power Supply 3.3V ϒ 5 %
19,30,36	VDD3	PWR	I/O Power Supply 3.3V ϒ 5 %
27	VDD4	PWR	I/O Power Supply 3.3V ϒ 5 %
48	VDDQ1	PWR	I/O Power Supply 2.5/3.3V ϒ 5 %
42	VDDQ2	PWR	I/O Power Supply 2.5/3.3V ϒ 5 %
3,9,16,22,33, 39,45	Vss	GND	Ground

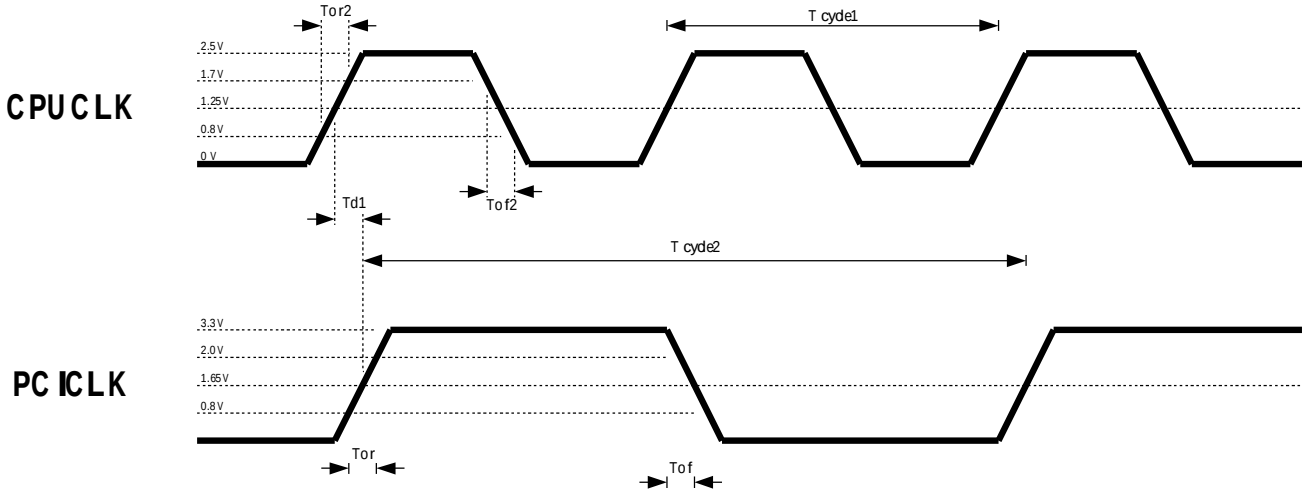
Mode control

Mode	SDRAM10/PCI_STOP#
0	PCI_STOP#
1	SDRAM10

Mode is selected during Power-on latching.

Electrical Characteristics

Characteristics	Symbol	Conditions	Mix	Type	Max	Unit
Output rise time (20pf Load)	Tor	From 0.8V to 2.0V,Vdd=3.3V			2.0	ns
Output fall time (20pf Load)	Tof	From 2.0V to 0.8V,Vdd=3.3V			2.0	ns
Output rise time (20pf Load)	Tor2	From 0.7V to 1.7V,Vdd=2.5V			1.0	ns
Output fall time (20pf Load)	Tof2	From 1.7V to 0.7V,Vdd=2.5V			1.0	ns
Duty cycle (20pf Load, at 1.5V)	Tduty	CPU, PCICLK	45	50	55	%
Clock Skew (20pf Load, at 1.5V)	Tskw1	CPUCLK to CPUCLK			250	ps
Clock Skew (20pf Load, at 1.5V)	Tskw2	PCICLK to PCICLK			300	ps
CPUCLK To PCICLK Delay	Td1	CUPCLK Leads	1	2	4	ns
Jitter, Absolute (20pf Load)	Tj1	CPUCLK, SDRAM			300	ps
Jitter, Absolute (20pf Load)	Tj2	PCICLK			300	ps



RTM520-39 Control Register Definitions:

When SCLK is pulled high during Power-on, I²C function will turn on.

1. I²C slave base address:

D2H

2. I²C Control Register:

CR00h : (default 00h)

Bit7:	0	ϒ1.5% Spectrum Modulation	
	1	ϒ0.5% Spectrum Modulation	
Bit[6.5.4]		CPU/SDRAM	PCI(Sync=1 \ 0)
0 0 0		124	41.3
0 0 1		75	37.5
0 1 0		83.3	417
0 1 1		68.8	33.4
1 0 0		103	34.3
1 0 1		112	37.3
1 1 0		**133.3**	**33.3(Programmable)**
1 1 1		100	33.3
Bit3:	0	Frequency selection disable	
	1	Frequency selection enables	
Bit2:	0	Center Modulation	
	1	Down Modulation	
Bit1:	0	Normal Output (default)	
	1	Spectrum Modulation Enable	
Bit0:	0	Running	
	1	Tri-state all outputs	

CR01h : (default ffh)

Bit[0 .. 1]	CPUCLK[0 .. 1] enable/stopped (1 = enable, 0 = stopped)
Bit[2 .. 3]	SDRAM[13 .. 12] enable/stopped (1 = enable, 0 = stopped)
Bit[4 .. 7]	Reserved

CR02h : (default ffh)

Bit[0 .. 4]	PCICLK[0 .. 4] enable/stopped (1 = enable, 0 = stopped)
Bit5:	Reserved
Bit6:	PCICLK_F enable/stopped (1 = enable, 0 = stopped)
Bit7:	Reserved

CR03h : (default ffh)

Bit0:	SDRAMCLK[0 .. 3] enable/stopped (1 = enable, 0 = stopped)
Bit1:	SDRAMCLK[4 .. 7] enable/stopped (1 = enable, 0 = stopped)
Bit2:	SDRAMCLK[8 ..11] enable/stopped (1 = enable, 0 = stopped)
Bit3:	Reserved
Bit4:	48MHz enable/stopped (1 = enable, 0 = stopped)
Bit5:	24MHz enable/stopped (1 = enable, 0 = stopped)
Bit6:	Reserved
Bit7:	Reserved

CR04h : (default ffh)

Bit[0 .. 7]:	Reserved

CR05h : (default ffh)

Bit[0 .. 1]	REF[[0 .. 1] enable/stopped (1 = enable, 0 = stopped)
Bit[3 .. 2]	Reserved
Bit4	IOAPIC enable/stopped (1 = enable, 0 = stopped)
Bit[7 .. 5]	Reserved

CR06h : (default ffh)

Bit[0 .. 7]	Reserved for test

CR07h .. CR0fh : (default ffh)

All Registers Reserved.

Power management of Clock Synthesizer

Power Down Control:

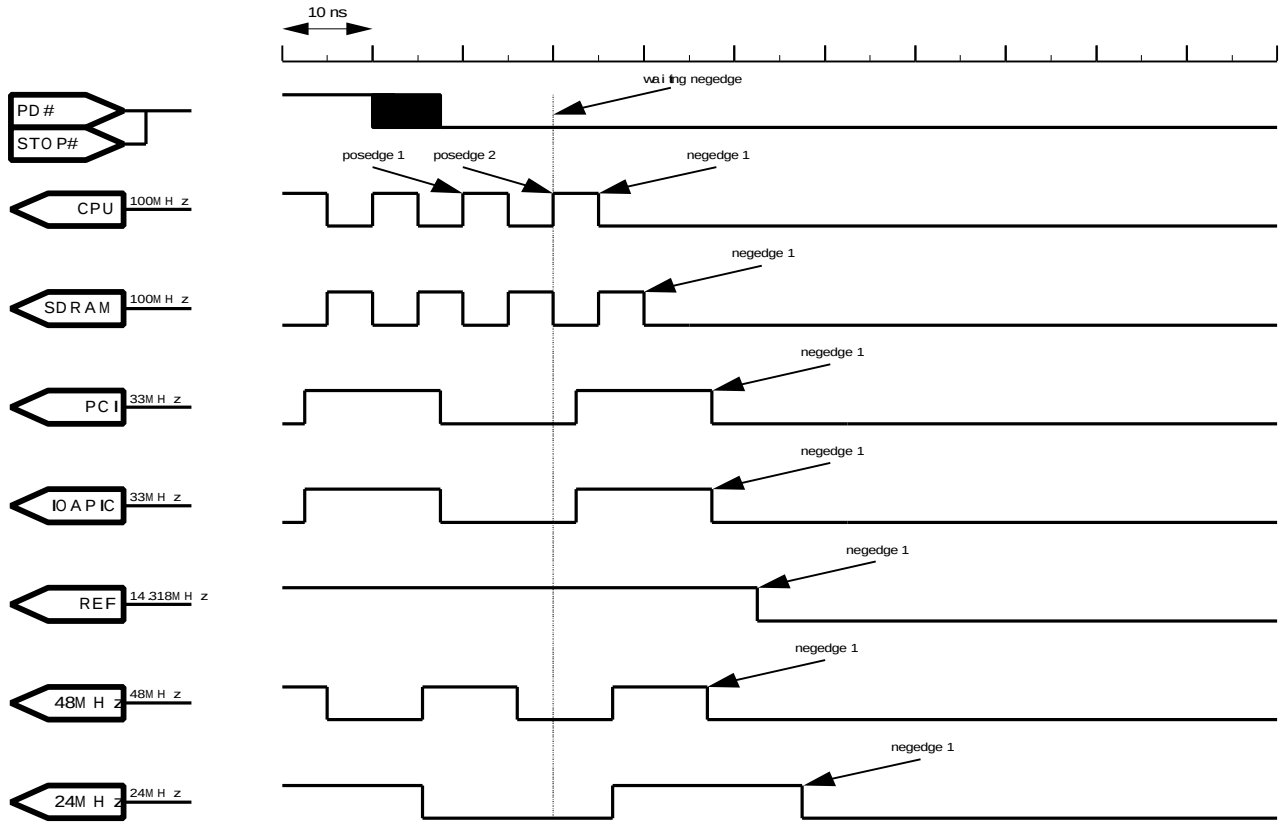
The power down selection is used to switch into a low power state. When PW_DN# is active low, all clocks need to be driven to a low state and held prior to turning off the VCO and Crystal. The PCI_STOP# and CPU_STOP# are considered to be do not care during the power down operations.

CPU Clock Stop Control:

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. The CPU and SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width to be a full pulse.

PCI Clock Stop Control:

PCI_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the PCI clocks for low power operation. The PCI clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width to be a full pulse.

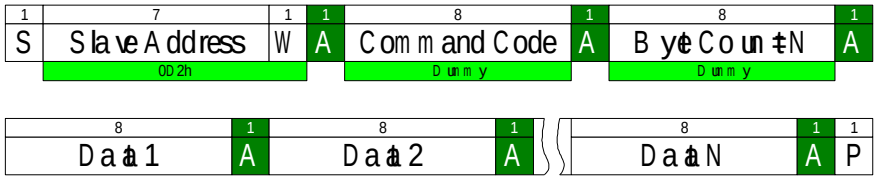


I²C Serial Bus Control:

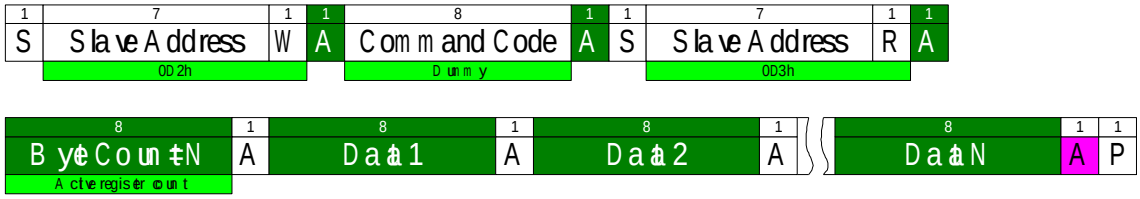
Support System management bus block-mode and word-mode.

Refer standard I²C and System management bus specification 1.0.

The Block mode:



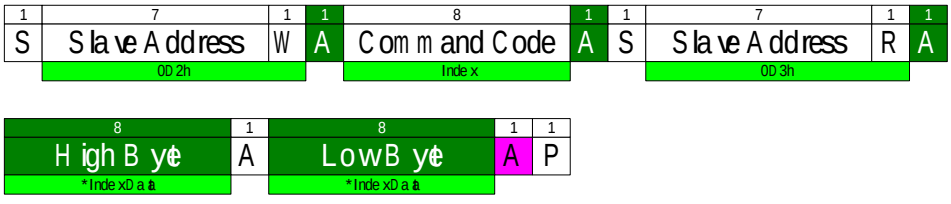
Block Write



Block Read

The Word mode:

Write Word



Read Word

Note slave address is D2h.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD} , V_{IN}	Supply Voltage	0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	^{0}C
T_A	Ambient Operating Temperature	0 to+70	^{0}C

Stresses exceeding those listed under Absolute Maximum Ratings may cause permanent damage to the device. These represent a stress rating only. Functional operation of the device at these or any other conditions exceeding those listed in the operational sections of the specifications in not implied. Maximum conditions for extended periods may affect product reliability.

DC Electrical Characteristics

T_A=0~70^{0}C, Supply voltage V_{DD}= V_{DDL}=3.3V+/-5%(unless otherwise specified)

*T_A=0~70^{0}C, Supply voltage V_{DD}= V_{DDL}=3.3V+/-5%,V_{DDL}=2.5V+/-5%

Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Input High Voltage	V_{IH}		2		V_{DD+}0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL}	V_{IN}=0V; Inputs with no pull-up	-5	2		µA
Operating Supply	$I_{DD3.3OP}$	C_L=0pF; Select @ 66MHz		100	160	mA
Current	$I_{DD2.5OP}$*	C_L=0pF;Select @66.9 MHz*		8	20	mA
Input Frequency	F_I	V_{DD}= 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time	T_{rans}	To 1st crossing of target Freq.			2	ms
Clk Stabilization	T_{STAB}	From V_{DD}=3.3 V to 1% target Freq.			2	ms
Skew	$t_{CPU-SDRAM1}$	V_T=1.5V			500	ps
	$t_{CPU-PCI1}$	V_T=1.5V	1	26	4	ns
	$t_{CPU-SDRAM2}$*	V_T=1.5V;V_{TL}=1.25V*			800	ps
	$t_{CPU-PCI2}$*	V_T=1.5V;V_{TL}=1.25V*	1		4	ps

AC Electrical Characteristics- CPU

T_A=0-70^{0}C; V_{DD}=3.3V+/-5%, V_{DDL}=2.5V+/-5%; C_L=20pF

Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Output Impedance	R_{DSP2B}	V_O= V_{DD}*(0.5)	13.5		45	Ohm
Output Impedance	R_{DSN2B}	V_O= V_{DD}*(0.5)	13.5		45	Ohm
Output High Voltage	V_{OH2B}	I_{OH}=-8mA	2	2.2		V
Output Low Voltage	V_{OL2B}	I_{OL}=12mA		0.3	0.4	V
Output High Current	I_{OH2B}	V_{OH}=1.7V		-20	-16	mA
Output Low Current	I_{OL2B}	V_{OL}=0.7V	19	26		mA
Rise Time	t_{r2B}	V_{OL}=0.4V, V_{OH}=2.0V		2.2	2.5	ns
Fall Time	t_{f2B}	V_{OH}=2.0V, V_{OL}=0.4V		1.1	1.6	ns
Duty Cycle	d_{t2b}	V_T=1.25V	45		55	%
Skew	t_{sk2B}	V_T=1.25V			250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$	V_T=1.25V		200	400	ps
Jitter, One Sigma	t_{j1s2B}	V_T=1.25V		50	150	ps
Jitter, Absolute	t_{jabs2B}	V_T=1.25V	-300		300	ps

AC Electrical Characteristics- PCI

T_A=0-70^{0}C; V_{DD}=3.3V+/-5%; C_L=30pF

Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Output Impedance	R_{DSP1}	V_O= V_{DD}*(0.5)	10		24	Ohm
Output Impedance	R_{DSN1}	V_O= V_{DD}*(0.5)	10		24	Ohm
Output High Voltage	V_{OH1}	I_{OH}=-28mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL}=23mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH}=2.0V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL}=0.8V	41	50		mA
Rise Time	t_{r1}	V_{OL}=0.4V, V_{OH}=2.4V		1.6	2	ns
Fall Time	t_{f1}	V_{OH}=2.4V, V_{OL}=0.4V		1.2	2	ns
Duty Cycle	d_{t1}	V_T=1.5V	45	51	55	%
Skew	t_{sk1}	V_T=1.5V		100	250	ps
Jitter, One Sigma	t_{j1s1} t_{j1s1a}	V_T=1.5V, synchronous V_T=1.5V, asynchronous		100 200	300 400	ps
Jitter, Absolute	t_{jabs1} t_{jabs1a}	V_T=1.5V, synchronous V_T=1.5V, asynchronous	-500 -1000		500 1000	ps ps

AC Electrical Characteristics- SDRAM

T_A=0-70^{0}C; V_{DD}=3.3V+/-5%; C_L=30pF

Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Output Impedance	R_{DSP1}	$V_O=V_{DD}*(0.5)$	10		24	Ohm
Output Impedance	R_{DSN1}	$V_O=V_{DD}*(0.5)$	10		24	Ohm
Output High Voltage	V_{OH1}	I_{OH}=-28mA	2.4	3		V
Output Low Voltage	V_{OL1}	I_{OL}=23mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH}=2.0V		-60	-40	mA
Output Low Current	I_{OL1}	V_{OL}=0.8V	41	50		mA
Rise Time	T_{r1}	V_{OL}=0.4V, V_{OH}=2.4V		1.6	2	ns
Fall Time	T_{f1}	V_{OH}=2.4V, V_{OL}=0.4V		1.2	2	ns
Duty Cycle	D_{t1}	V_T=1.5V	45	52	55	%
Skew	T_{sk1}	V_T=1.5V		150	250	ps
Jitter, One Sigma	T_{j1s1}	V_T=1.5V		50	150	ps
Jitter, Absolute	T_{jabs1}	V_T=1.5V	-250		+250	ps

AC Electrical Characteristics-IOAPIC

T_A=0-70^{0}C; V_{DD}=3.3V+/-5%, V_{DDL}=2.5V+/-5%; C_L=20pF

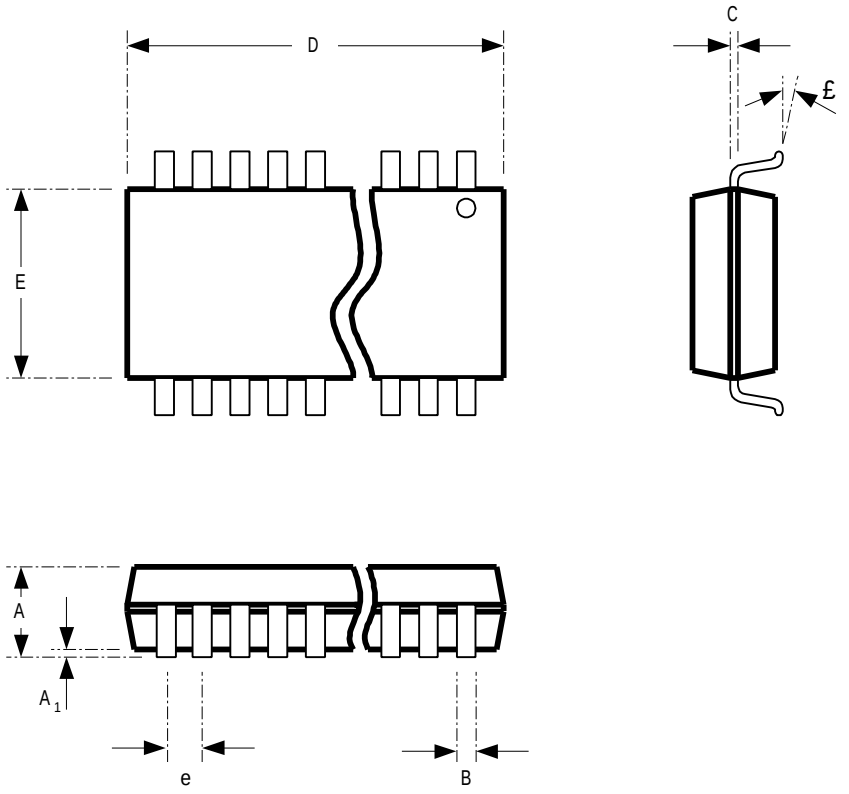
Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Output Impedance	R_{DSP4B}	$V_O=V_{DD}*(0.5)$	13.5		45	Ohm
Output Impedance	R_{DSN4B}	$V_O=V_{DD}*(0.5)$	13.5		45	Ohm
Output High Voltage	V_{OH4B}	I_{OH}=-8mA	2	2.2		V
Output Low Voltage	V_{OL4B}	I_{OL}=12mA		0.3	0.4	V
Output High Current	I_{OH4B}	V_{OH}=1.7V		-20	-16	mA
Output Low Current	I_{OL4B}	V_{OL}=0.7V	19	26		mA
Rise Time	T_{r2B}	V_{OL}=0.4V, V_{OH}=2.0V		1.4	1.7	ns
Fall Time	T_{f2B}	V_{OH}=2.0V, V_{OL}=0.4V		1.3	1.6	ns
Duty Cycle	D_{t2b}	V_T=1.25V	50		60	%
Jitter, One Sigma	T_{j1s2B}	V_T=1.25V		1	3	%
Jitter, Absolute	T_{jabs2B}	V_T=1.25V	-5		5	%

AC Electrical Characteristics- 24,48MHz, Ref(0:1)

T_A=0-70^{0}C; V_{DD}=V_{DDL}=3.3V+/-5%; C_L=10-20pF

Parameter	Symbol	Test Conditions	Min	Type	Max	Units
Output Impedance	R_{DSP5}	V_O=V_{DD}*(0.5)	20		60	Ohm
Output Impedance	R_{DSN5}	V_O=V_{DD}*(0.5)	20		60	Ohm
Output High Voltage	V_{OH5}	I_{OH}=-16mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL}=9mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH}=2.0V		-32	-22	mA
Output Low Current	I_{OL5}	V_{OL}=0.8V	16	25		mA
Rise Time	t_{r5}	V_{OL}=0.4V, V_{OH}=2.4V		1.7	4	ns
Fall Time	t_{f5}	V_{OH}=2.4V, V_{OL}=0.4V		1.6	4	ns
Duty Cycle	d_{t5}	V_T=1.5V	45	53	55	%
Jitter, One Sigma	t_{j1s5}	V_T=1.5V		1	3	%
Jitter, Absolute	t_{jabs5}	V_T=1.5V		3	8	%

Mechanical Package Outline



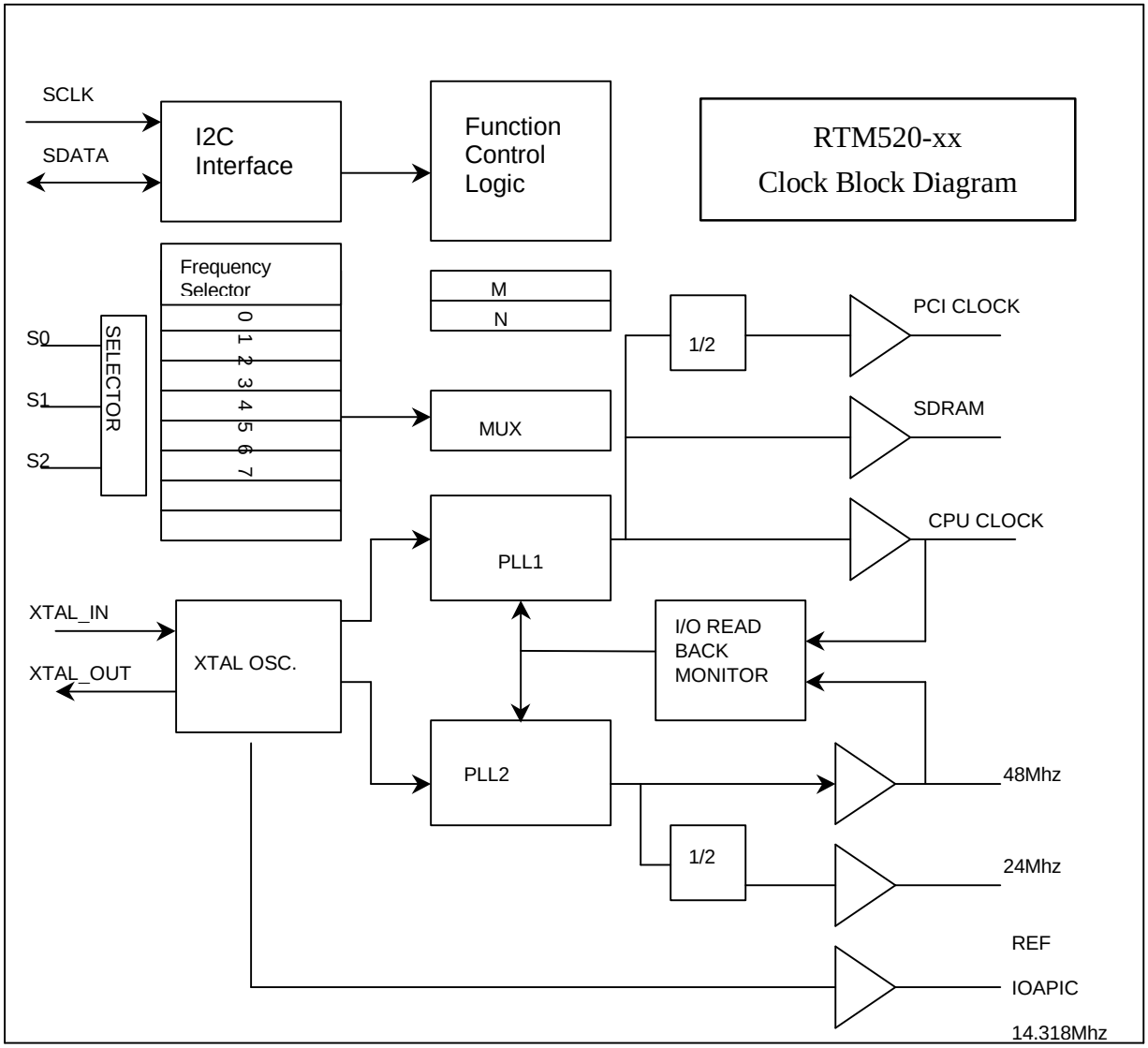
SSOP Package:(unit using inches)

Symbol	Common Dimensions			Variations	D			N
	Min.	Type	Max.		Min.	Type	Max.	
A	0.095	0.101	0.110	AC	0.620	0.625	0.630	48
A1	0.008	0.012	0.016	AD	0.720	0.725	0.730	56
B	0.008	0.010	0.0135					
C	0.005	0.0075	0.010					
D	See Variations							
E	0.292	0.296	0.299					
e	0.025BSC							
α	0′	5′	10′					

OVERVIEW

RTM520 represents a series of Realtek mother-board clock synthesizers designed based on the second generation Relaxation Oscillator architecture which delivers highly efficient and stable working frequency and effectively controls clock jittering. RTM520 provides output frequency above 200 Mhz for 3.3V and 5V operation. Based on Realtek years of experience in graphic and LAN products and volume delivery in excess of 10 million unit wise, RTM520 is capable of providing 2 sets of PLL(Phase Locked Loop) exceeding 200Mhz. One set of PLL provides synchronized timing sequential signal needed for CPU master clock and SDRAM with its working frequency ranging from 50Mhz to 166Mhz, and yet supports linear frequency modulation. Another set of PLL provides primarily the working frequency for system peripheral devices. With oscillating frequency at 96Mhz and the use of frequency divider, both 48Mhz and 24Mhz are available to provide frequency for USB & FDD devices.

RTM520 System Block Diagram:



RTM520 clock synthesizers exploit the ATPG design architecture with internal built snoop circuit to effectively monitor product characteristic and increase its yield and reliability. As shown in diagram, Read-Back Monitor will snoop clock synthesizer operational states in real time while the chip test mode being turned on.

RT Special Function

RTM520 clock synthesizer series effectively provides access to I2C Read/Write programming registers. Other than retaining the typical Clock Generator Block Access mode, setting the required register will allow standard I2C access to the RTM520 internal registers which in turn speeds the coding process for system developers.

RT Special Registers Definition

CR10h Miscellaneous register

Bit 0	0	RT I2C register write disable	
	1	RT I2C register write enable	
Bit 1	0	I2C read from index #0 (mode 0)	
	1	I2C read from previous index (mode 1)	
Bit[3..2]	Reserved		
Bit[7..4]	version ID	0000= A	
		0000= B	
		0010= C	
		0000= D	

CR11h Program M code for CPU/SDRAM clocks

Bit 7..0	M Code

CR12h Program N code for CPU/SDRAM clocks

Bit 7..0	N Code

f1= 14.318Mhz * (M+1) / (N+1)

CR13h Power down control register

Bit 0	0	CPU_STOP# active
	1	CPU clock free running
Bit 1	0	PCI_STOP# active
	1	PCI clock free running
Bit 2	0	Power down mode enable
	1	Normal operations
Bit 3	0	PCI=CPU/4 (default) [but version A not ready]
	1	PCI=CPU/3
	* only for select [110] programmable frequency	
Bit [7..3]	Reserved	

CR14h..19h Reserved for testing

CR1ah Chip status register

Bit 0..3	Reserved
Bit 7..4	Frequency selection at power on s3 s2 s1 s0

CR1fh Command Register

Bit 7..0	Write command, Load data from register buffer and then execute it

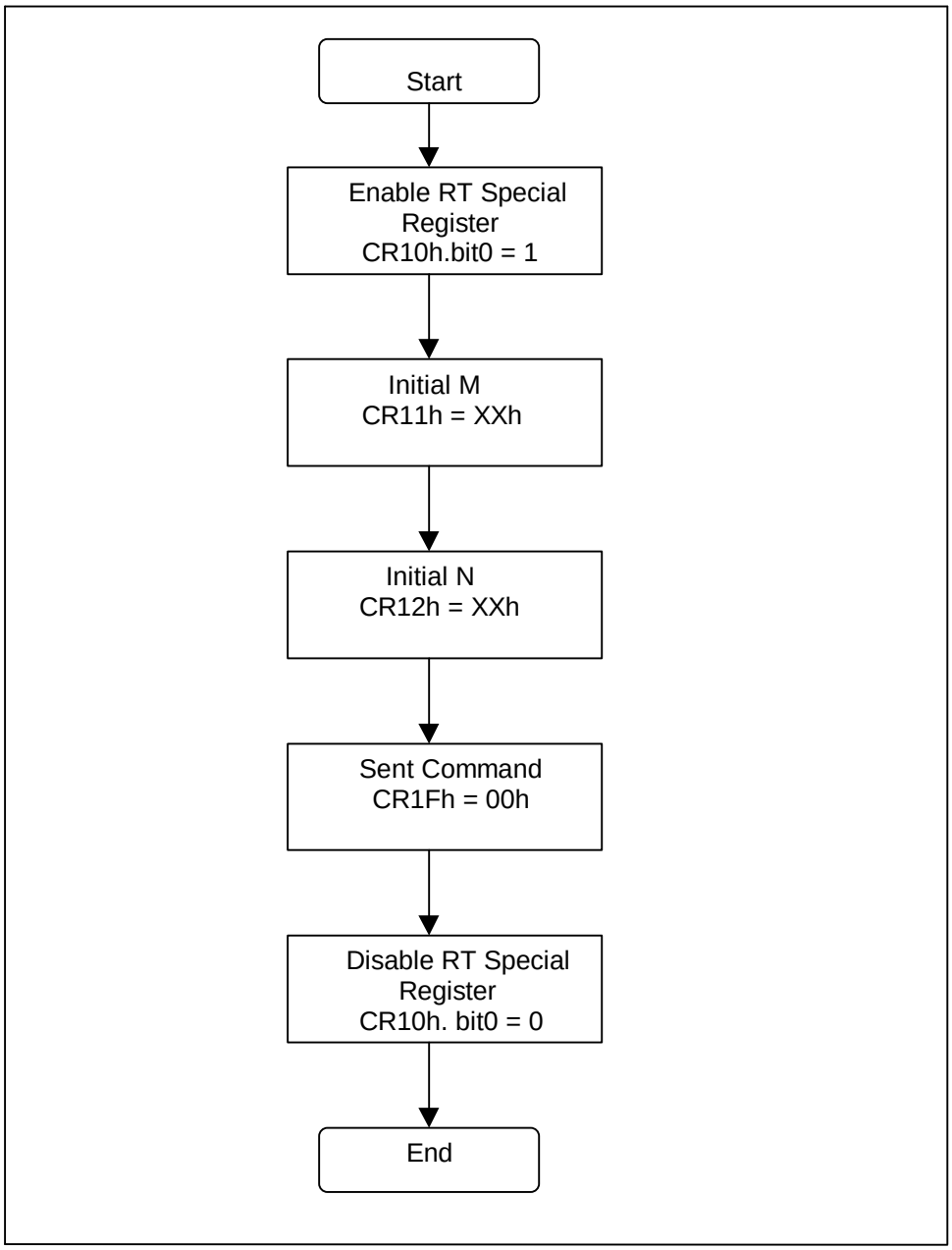
Programmable Frequency Guide

To provide pragmatic system board integration, RTM520 Clock Synthesizer series is equipped with equational PLL in which parameters (m, n) can be set to adjust CPU & SDRAM synchronized timing sequence. RTM520 supports frequency from 50Mhz to 133Mhz as well as smooth frequency change in accommodating top system performance. The synchronized output frequency is as followed:

1. F_{out} = [14.318Mhz * (m+1) / (n+1)]

   Note: Refer to Appendix A for Frequency Table

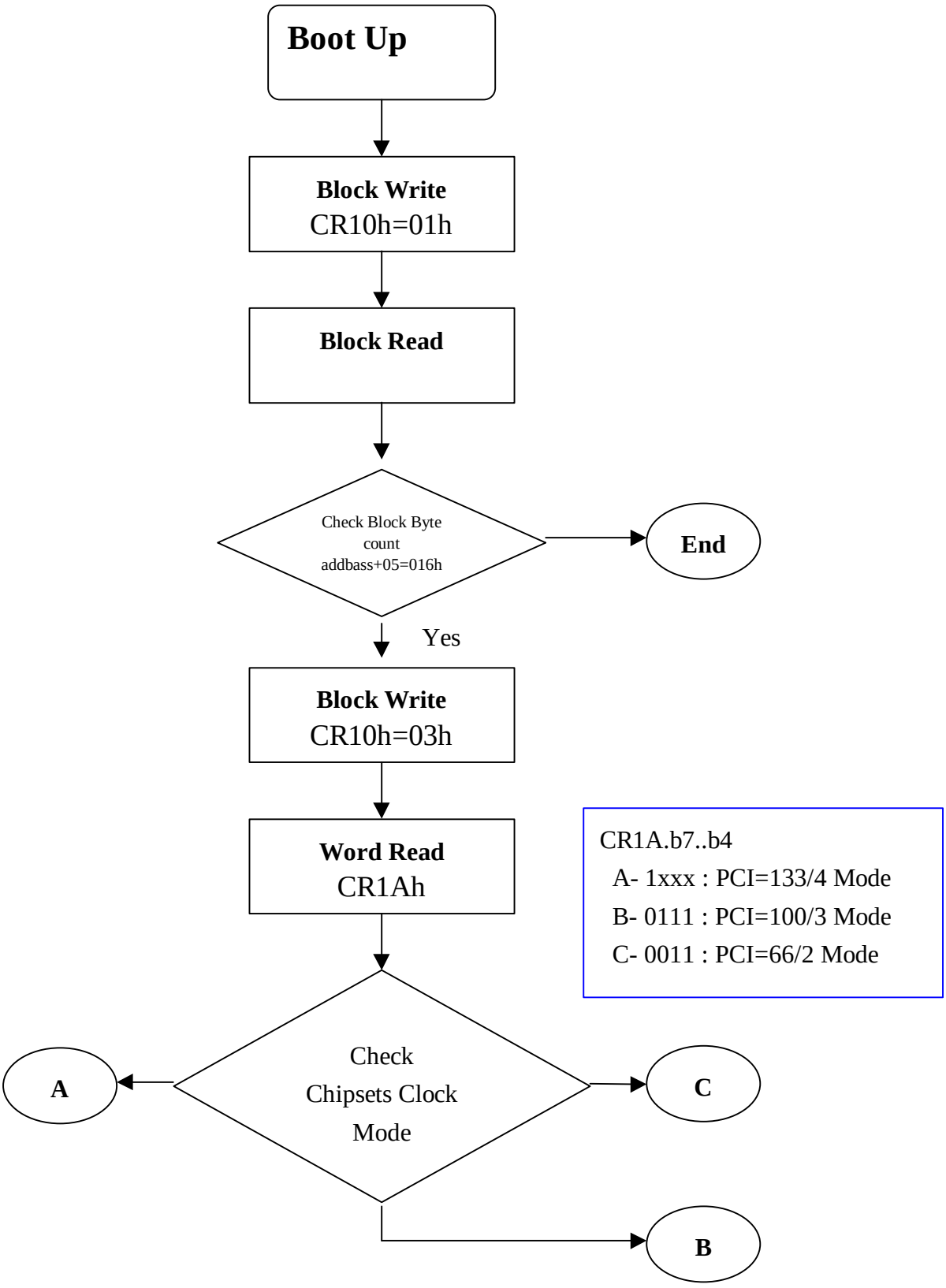
Programming Flow Chart:

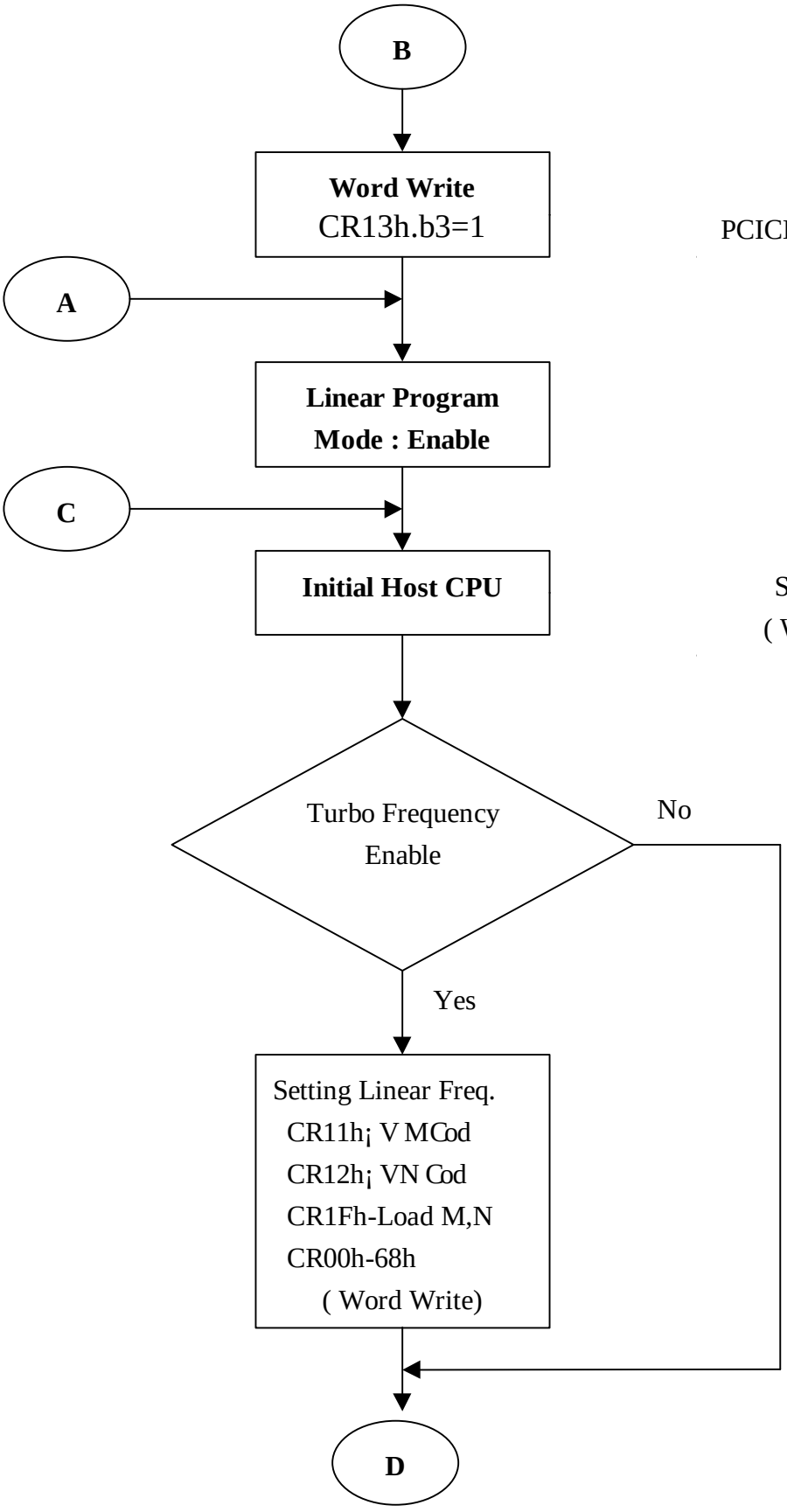


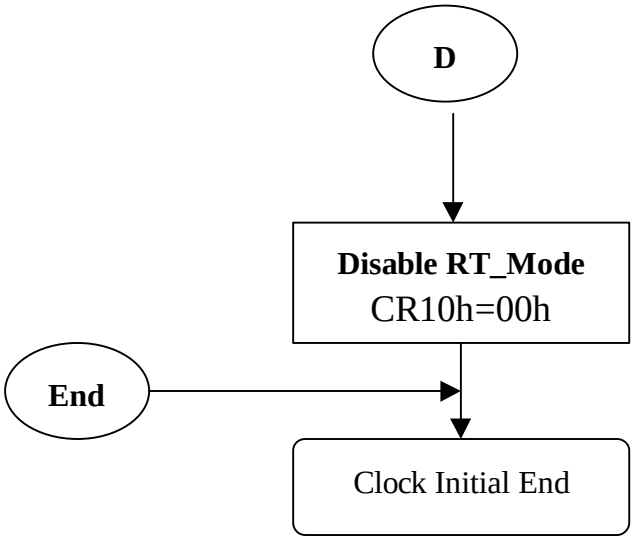
RTM520-39 frequency table1

N (DEC.)	M (HEX.)	M (DEC.)	Frequency (MHZ)	N (DEC.)	M (HEX.)	M (DEC.)	Frequency (MHZ)
15	32 h	50	45.64	15	6E h	110	99.33
15	33 h	51	46.53	15	6F h	111	100.23
15	34 h	52	47.43	15	70 h	112	101.12
15	35 h	53	48.32	15	71 h	113	102.02
15	36 h	54	49.22	15	72 h	114	102.91
15	37 h	55	50.11	15	73 h	115	103.81
15	38 h	56	51.01	15	74 h	116	104.70
15	39 h	57	51.90	15	75 h	117	105.60
15	3A h	58	52.80	15	76 h	118	106.49
15	3B h	59	53.69	15	77 h	119	107.39
15	3C h	60	54.59	15	78 h	120	108.28
15	3D h	61	55.48	15	79 h	121	109.17
15	3E h	62	56.38	15	7A h	122	110.07
15	3F h	63	57.27	15	7B h	123	110.96
15	40 h	64	58.17	15	7C h	124	111.86
15	41 h	65	59.06	15	7D h	125	112.75
15	42 h	66	59.96	15	7E h	126	113.65
15	43 h	67	60.85	15	7F h	127	114.54
15	44 h	68	61.75	15	80 h	128	115.44
15	45 h	69	62.64	15	81 h	129	116.33
15	46 h	70	63.54	15	82 h	130	117.23
15	47 h	71	64.43	15	83 h	131	118.12
15	48 h	72	65.33	15	84 h	132	119.02
15	49 h	73	66.22	15	85 h	133	119.91
15	4A h	74	67.12	15	86 h	134	120.81
15	4B h	75	68.01	15	87 h	135	121.70
15	4C h	76	68.91	15	88 h	136	122.60
15	4D h	77	69.80	15	89 h	137	123.49
15	4E h	78	70.70	15	8A h	138	124.39
15	4F h	79	71.59	15	8B h	139	125.28
15	50 h	80	72.48	15	8C h	140	126.18
15	51 h	81	73.38	15	8D h	141	127.07
15	52 h	82	74.27	15	8E h	142	127.97
15	53 h	83	75.17	15	8F h	143	128.86
15	54 h	84	76.06	15	90 h	144	129.76
15	55 h	85	76.96	15	91 h	145	130.65
15	56 h	86	77.85	15	92 h	146	131.55
15	57 h	87	78.75	15	93 h	147	132.44
15	58 h	88	79.64	15	94 h	148	133.34
15	59 h	89	80.54	15	95 h	149	134.23
15	5A h	90	81.43	15	96 h	150	135.13
15	5B h	91	82.33	15	97 h	151	136.02
15	5C h	92	83.22	15	98 h	152	136.92
15	5D h	93	84.12	15	99 h	153	137.81
15	5E h	94	85.01	15	9A h	154	138.71
15	5F h	95	85.91	15	9B h	155	139.60
15	60 h	96	86.80	15	9C h	156	140.50
15	61 h	97	87.70	15	9D h	157	141.39
15	62 h	98	88.59	15	9E h	158	142.29
15	63 h	99	89.49	15	9F h	159	143.18
15	64 h	100	90.38	15	A0 h	160	144.07
15	65 h	101	91.28	15	A1 h	161	144.97
15	66 h	102	92.17	15	A2 h	162	145.86
15	67 h	103	93.07	15	A3 h	163	146.76
15	68 h	104	93.96	15	A4 h	164	147.65
15	69 h	105	94.86	15	A5 h	165	148.55
15	6A h	106	95.75	15	A6 h	166	149.44
15	6B h	107	96.65	15	A7 h	167	150.34
15	6C h	108	97.54	15	A8 h	168	151.23
15	6D h	109	98.44	15	A9 h	169	152.13

RTM520-39C Initial Notice For VIA Apollo (133Mhz FSB)




B
Word Write
CR13h.b3=1
Setting
PCICLK=CPUCLK/4
A
Linear Program
Mode : Enable
C
Initial Host CPU
Setting CR0
(Word Write)
Turbo Frequency
Enable
No
Yes
Setting Linear Freq.
CR11h¡ V MCod
CR12h¡ VN Cod
CR1Fh-Load M,N
CR00h-68h
(Word Write)
D


D
Disable RT_Mode
CR10h=00h
End
Clock Initial End

DEMO board schematic